REMARKS

Claims 1 to 14 are now pending and being considered.

It is respectfully submitted that all of the presently pending claims are allowable, and reconsideration is respectfully requested.

As to the general and unsupported assertions regarding the adequacy of the prior response. It is respectfully submitted that the prior response absolutely conforms to Rule 111 and did represent a fully adequate response, as evidenced by the fact that the Office has withdrawn the prior rejections and a number of the prior references. As to paragraph five (5) of the Final Office Action, it suggests that the dependent claims were not adequately argued as to patentability. It is particularly noted that the Final Office Action's "analysis" of the adequacy of the prior response wholly ignored the fact that these dependent claims included all of the features of their base independent claims -- *which themselves were plainly distinguished as to why they were specifically patentable over the references relied upon in the prior Office Action.* In particular, the prior response included *extensive and detailed reasoning* as to why the base claims were distinguishable over the applied references (see pages six (6), seven (7), eight (8) and nine (9) of the prior Response). It is fundamentally axiomatic that a dependent claim is allowable for the same reasons as its base claim, where none of the non-primary references cure the critical deficiencies of the primary references as applied. It is therefore not necessary to further argue any further features of the dependent claims, where such claims are allowable as a result of the allowability of their base claims, as was the case in the prior response.

With respect to paragraph seven (7), claims 1 to 4, 7, 8, and 10 to 14 were rejected under 35 U.S.C. § 103(a) as unpatentable over the purported "admitted prior art" in view of U.S. Patent No. 6,502,209 ("Bengtsson") -- and in further view of the newly applied third-level reference of JP 405173890A to Weikmann.

It is first noted that the third-level Hollander et al., U.S. Patent No. 6,412,071 from the prior Office Action has been dropped in view of the prior Response).

Applicants first note that the Final Office Action relies on the BACKGROUND INFORMATION Section of the present application. In this regard, it is noted that while certain published information may represent prior art (namely, any cited patents that are prior

art), it is believed and respectfully submitted that the information concerning the "debug logic triggering" represents the internal and unpublished knowledge of Bosch. In particular, *nowhere* in the present application is the "debug logic triggering" information admitted to be prior art. Accordingly, it is respectfully submitted that the obviousness assertions are not sustainable for this reason alone.

In rejecting a claim under 35 U.S.C. § 103(a), the Examiner bears the initial burden of presenting a *prima facie* case of obviousness. In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). To establish prima facie obviousness, three criteria must be satisfied. First, there must be some suggestion or motivation to modify or combine reference teachings. In re Fine, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). This teaching or suggestion to make the claimed combination must be found in the prior art and not based on the application disclosure. In re Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Second, there must be a reasonable expectation of success. In re Merck & Co., Inc., 800 F.2d 1091, 231 U.S.P.Q. 375 (Fed. Cir. 1986). Third, the prior art reference(s) must teach or suggest all of the claim features. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974).

While the rejections may not be agreed with in view of all of the foregoing , to facilitate matters, claims 1, 10 and 13 as presented provide that "*the debug logic and its registers are operated in parallel to the program execution time to check a stack having the specific address range and an exception routine is set up in reaction to a break point event in the stack., so as to provide a secure stack check without using the program execution time of the microcontroller*".

First, as regards the background of the presently claimed subject matter, the problem with regard to modern RISC machines is that it is not adequate to write into the single memory cell a pattern because of the fact that by building a stack frame of a function the jump over more than one address takes place. Not all the addresses which are jumped over have to be changed in reality. With regard to the width of the region which has to be covered by a pattern the program time which is necessary to check the pattern increases. With regard to the presently claimed subject matter, the program region which should be checked is defined in a stack. To check the stack parallel to operating time a memory region at the bottom of the stack is defined whereby the width is defined by the maximum gap which could arise because of the alignment of variables. This memory region or stack is then secured by a

break point condition in debug registers (range break). These registers and the logic behind are normally meant for debugging and are not used parallel to operating or execution time. So in the context of the presently claimed subject matter, this debug logic and the registers are used parallel to the operating or execution time to check the stack and, in reaction to a break point event in that stack, an exception routine (for instance, a recovery mechanism) is set up, so that there is a secure stack check without using the program time of the CPU.

The secondary Bengtsson reference only refers to a computer chip which is settable in two different modes, a DUT mode and a monitor mode. What Bengtsson concerns is a setting (column 2 line 52 to 53), a full rate debugging obtaining full information about the program execution. So Bengtsson concerns the time before a normal operation of the debug logic as explained in the background information. The Bengtsson et al. document does not in any way disclose or show more than this, and in particular the Bengtsson reference does not in any way show or disclose the parallel monitoring by using the debug logic in normal operation of the program.

As to the third-level Weikmann reference, it only concerns a data protecting microprocessor circuit for portable record carriers for example credit cards. In the Weikmann reference, the address W is put in register 22 and register 24 and it is compared with the contents of the address register 124. If it is smaller than W in register 22, this means that the secondary program uses a memory region between 0 and W-1 which is not allowed because the secondary program starts with address W. *What is not shown or otherwise disclosed* in the Weikmann reference, whether taken alone or combined, is the feature of "causing the debug logic to trigger an exception upon access to a specific address range during a program execution time" and the feature of accessing the specific address range to include access to an illegal storage area. So this combination that causing the debug logic to trigger an exception upon access to a specific address range wherein access to an illegal storage area is included is not in any way shown or disclosed in the Weikmann reference, whether taken alone or combined.

Also, as previously explained, in the context of the presently claimed subject matter, the controller already has debug registers and an existing debug functionality. These debug registers and the logic behind this functionality is only used for debugging and not for the normal operation of the control unit. In the normal operation of the control unit, these registers, the respective logic and the respective functionality for debugging is not used in the

known state of the art. *The claimed subject matter is directed to using these registers and the respective logic and the respective debug functionality for monitoring the microcomputer without absorbing runtime and resources of the CPU.* This benefit is nowhere provided by the applied patent references.

This is realized as described at page 7 of the present application in that way that the debug logic monitor whether the program accesses an address range of the stack of the microcontroller beyond a pre-selected able maximum stack size. Beyond this maximum stack size an illegal storage area known as a break region is defined on which a break point is set. If a stack pointer points to this illegal storage area during the program execution time, i.e., if an attempt is made *to access the illegal storage area,* an exception is triggered. So for monitoring the stack with regard to runtime a memory area or stack area at the lower end of the stack is defined. The size of this area is defined by the maximum lack or space which could come up with regard to alignment of variables on the stack. This memory or stack area is secured by a break point condition in the debug registers (range-break). In reaction to the break point event it is branched into exception routine which could be handled by using a suitable exception handling, for example, a recovery mechanism. By using this method a secure stack monitoring is obtained without absorbing runtime of the CPU which has no increase of its workload.

In the context of the presently claimed subject matter, the unused debug functionality is used in normal operation. The "Bengtsson" reference indicates normal usage of a debug hardware and a debug system within a debug mode -- and not in normal operation.

With the presently claimed subject matter, as provided at page 7 (first paragraph) of the present application, as to the illegal memory area, a break region is defined on which there is a break point. Accordingly, with the presently claimed subject matter, it is a condition for an exception handling if the stack pointer points to this illegal memory area, as provided for in the context of claims 1, 10 and 13 as presented.

The "Bengtsson" reference refers to the development of a debug-supplement to provide for the possibility to debug systems with a cache memory. This is the normal usage of a debug hardware in the real and concrete meaning of the word debugging.

In contrast, the claimed subject matter concerns the usage of an already existing debug functionality of the microcomputer to realize a monitoring of the stack memory. With this background a secure monitoring of the microcomputer is possible without absorbing run-time and resources of the CPU. So the presently claimed subject matter does not describe the

conception, design or development of a debug logic for a microcomputer, but the usage of this for debugging normally used hardware in the software of the microcomputer itself when the microcomputer is in operation and not in debug mode. This is described in the specification on page 5, line 10 to line 17 and from line 19 to 23 on the same page and also on page 10, line 23 to page 11, line 10. This difference is also valid for the Figures 2 and 3 of the present application.

Still further, claims 1, 10, and 13, as presented, provide for monitoring *an execution of a program* that is executable on at least one microprocessor of a micro controller using a debug logic of the micro controller such that the *debug logic triggers an exception upon access to a specific address range during a program execution time,* the at least one microprocessor configures the debug logic, and the debug logic executes an exception routine *after the exception is triggered during the program execution time.* Furthermore, claims 1, 10, and 13 provide that the access to the specific address range includes ***access to an illegal storage area.***

In contrast, the background information discussed in specification states that "[i]n the methods known from the related art, only legal accesses to the I/O ports are handled. In the framework of the known methods, the commands and/or the program are not monitored for possible faults. The known method therefore simply involves an expansion of the operating system." (See Specification, page 4, lines 6 to 9).

Accordingly, this does not disclose or even suggest the feature of a debug logic triggering an exception upon access to a specific address range during a program execution time and executing an exception routine after the exception is triggered during the program execution time such that the access to the specific address range includes access to an illegal storage area, *in which the debug logic and its registers are operated in parallel to the program execution time to check a stack having the specific address range and an exception routine is set up in reaction to a break point event in the stack., so as to provide a secure stack check without using the program execution time of the microcontroller,* as provided for in the context of each of claims 1, 10 and 13 as presented

The background information merely indicates that only accesses to the I/O ports are handled such that commands and/or programs are not monitored for possible faults. Nothing in the background information discloses (or suggests) the features a debug logic triggering an exception upon access to a specific address range during a program execution time and

executing an exception routine after the exception is triggered during the program execution time such that the access to the specific address range includes access to an illegal storage area, *in which the debug logic and its registers are operated in parallel to the program execution time to check a stack having the specific address range and an exception routine is set up in reaction to a break point event in the stack., so as to provide a secure stack check without using the program execution time of the microcontroller*, as provided for in the context of claims 1, 10, and 13, as presented.

Additionally, the Office Action asserts that while the "[a]dmitted prior art does not explicitly disclose causing the at least one microprocessor to configure the debug logic", the "Bengtsson" reference "discloses in an analogous computer system the debug chip is configured in DUT (device under test)". (Office Action, page 4).

The "Bengtsson" reference concerns "a computer chip having integrated thereon a CPU and a cache system being interconnected, and at least one synchronization unit, said chip being [settable] in either one of at least two different running modes, a first one thereof being a device under test (DUT) mode, and a second one thereof being a MONITOR mode" and "[t]he chip further comprises a debug bus connectable to another identical chip for communicating signals enabling the chip and said another chip to run in parallel while said chips are set in complementary modes." (Col. 2, lines 32 to 43). Furthermore, the "Bengtsson" reference states that a "computer system 98 includes a chip 110C in DUT mode" and "[t]he monitor 100 includes two chips with enhanced debug capability 110A-B configured in MONITOR mode." (Col. 3, lines 54 to 65).

The "Bengtsson" reference further states that "a debug bus 140 is coupled to all chips 110A-C for synchronizing their activity including: power-on-reset, interrupts, wait states, DMA accesses and other asynchronous events" and that "only the debug chip 110C configured in DUT mode has its address line coupled to the address portion 146 of the system bus 146-148" such that debug chip 110C "acts as the master of the address portion of the system bus" and "determines what access requests will be handled on the address bus and therefore what data and or program code will be present on the data portion 148 of the system bus." Also, the "Bengtsson" references states that "[a] typical program sequence provided over the data portion of the system bus to each of the chips 110A-C might include a read or write instruction to a specific address followed by data being read from or written to that specific address by each of the above-mentioned chips" and that "[e]ach of the MONITOR mode chips 110A-B therefore shadows the activity of the master chip 110C receiving

identical data and instructions and performing the same operations 170C in response, for example, to the program code 180 stored in main memory" such that "[n]one of the monitor chips write to external memory 114" and "[t]he external memory is always written to only by the DUT mode debug chip 110C." (Col. 4, lines 21 to 56).

Accordingly, the "Bengtsson" reference does not disclose or even suggest the feature of a debug logic triggering an exception upon access to a specific address range during a program execution time and executing an exception routine after the exception is triggered during the program execution time such that the access to the specific address range includes access to an illegal storage area. The "Bengtsson" reference merely indicates that a debug chip is the master of an address portion of a system bus and it determines what access requests will be handled on the address bus and what data and/or program code will be present on a data portion of the system bus.

Nothing in the "Bengtsson" reference, whether taken alone or combined, discloses or suggests the feature of a debug logic triggering an exception upon access to a specific address range during a program execution time and executing an exception routine after the exception is triggered during the program execution time such that the access to the specific address range includes access to an illegal storage area, in which *the debug logic and its registers are operated in parallel to the program execution time to check a stack having the specific address range and an exception routine is set up in reaction to a break point event in the stack., so as to provide a secure stack check without using the program execution time of the microcontroller*", as provided for in the context of claims 1, 10, and 13, as presented.

Furthermore, the Office Actions to date only conclusorily assert that "it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of configuring the microprocessor or DUT to debug logic as taught by Bengtsson in to the method of monitoring the program as taught in admitted prior art."

Still further, it is respectfully submitted that the cases of In re Fine, supra, and In re Jones, 21 U.S.P.Q.2d 1941 (Fed. Cir. 1992), make plain that the Office Action's generalized assertions that it would have been obvious to modify or combine the references do not properly support a § 103 rejection. It is respectfully submitted that those cases make plain that the Office Action reflects a subjective "obvious to try" standard, and therefore does not

reflect the proper evidence to support an obviousness rejection based on the references relied

upon. In particular, the Court in the case of In re Fine stated that:

> The PTO has the burden under section 103 to establish a *prima
> facie* case of obviousness. It can satisfy this burden only by
> showing some objective teaching in the prior art or that knowledge
> generally available to one of ordinary skill in the art would lead
> that individual to combine the relevant teachings of the references.
> This it has not done. . . .
>
> **Instead, the Examiner relies on hindsight in reaching his
> obviousness determination. . . . One cannot use hindsight
> reconstruction to pick and choose among isolated
> disclosures
> in the prior art to deprecate the claimed invention.**

In re Fine, 5 U.S.P.Q.2d at 1598 to 1600 (citations omitted; italics in original; emphasis

added). Likewise, the Court in the case of In re Jones stated that:

> Before the PTO may combine the disclosures of two or more
> prior art references in order to establish *prima facie* obviousness,
> there must be some suggestion for doing so, found either in the
> references themselves or in the knowledge generally available to
> one of ordinary skill in the art. . . .
>
> **Conspicuously missing from this record is any evidence,
> other
> than the PTO's speculation (if it be called evidence) that one
> of ordinary skill . . . would have been motivated to make the
> modifications . . . necessary to arrive at the claimed [invention].**

In re Jones, 21 U.S.P.Q.2d at 1943, 1944 (citations omitted; italics in original).

That is exactly the case here since it is believed and respectfully submitted that the

Office Actions to date offer no evidence whatsoever, but only conclusory hindsight,

reconstruction and speculation, which these cases have indicated does not constitute evidence

that will support a proper obviousness finding. Unsupported assertions are not evidence as to

why a person having ordinary skill in the art would be motivated to modify or combine

references to provide the claimed subject matter of the claims to address the problems met

thereby. Accordingly, the Office must provide proper evidence of a motivation for

modifying or combining the references to provide the claimed subject matter.

More recently, the Federal Circuit in the case of In re Kotzab has made plain that even

if a claim concerns a "technologically simple concept" — which is not the case here — there

still must be some finding as to the "specific understanding or principle within the knowledge

of a skilled artisan" that would motivate a person having <u>no</u> knowledge of the claimed subject

matter to "make the combination in the manner claimed," stating that:

> In this case, the Examiner and the Board fell into the hindsight
> trap. The idea of a single sensor controlling multiple valves, as
> opposed to multiple sensors controlling multiple valves, is a
> technologically simple concept. <u>With this simple concept in mind,
> the Patent and Trademark Office found prior art statements that in
> the abstract appeared to suggest the claimed limitation. But, there
> was no finding as to the specific understanding or principle within
> the knowledge of a skilled artisan that would have motivated one
> with no knowledge of Kotzab's invention to make the combination
> in the manner claimed.</u> In light of our holding of the absence of a
> motivation to combine the teachings in Evans, we conclude that
> the Board did not make out a proper <u>prima facie</u> case of
> obviousness in rejecting [the] claims . . . under 35 U.S.C. Section
> 103(a) over Evans.

In re Kotzab, 55 U.S.P.Q.2d 1313, 1318 (Fed. Cir. 2000) (emphasis added). Here again,

there have been no such findings to establish that the features discussed above of the rejected

claims are met by the reference relied upon. As referred to above, any review of the

reference, whether taken alone or combined, makes plain that the reference simply does not

describe the features discussed above of the rejected claims.

It is therefore respectfully submitted that claims 1, 10, and 13 as presented are

allowable for these reasons. Claims 2 to 4, 7, and 8 depend on claim 1, and are therefore

allowable at least for the same reasons as claim 1. Claims 11 and 12 depend on claim 10, and

are therefore allowable at least for the same reasons as claim 10. Claims 14 depends on claim

13, and is therefore allowable at least for the same reasons as claim 13.

It is therefore respectfully submitted that the rejections of claims 1 to 4, 7, 8, and 10 to

14 should be withdrawn.

With respect to paragraph eight (8) of the Final Office Action, claims 5 and 6 were

rejected under 35 U.S.C. § 103(a) as unpatentable over the purported "admitted prior art"

(which as explained above is wrong as asserted) and the "Bengtsson" reference in view of

U.S. Patent No. 6,697,972 ("Oshima").

Claims 5 and 6 depend from allowable claim 1, as presented – and therefore include

all of the features of claim 1 as presented It is therefore respectfully requested that the

obviousness rejections be withdrawn since claims 5 and 6 are allowable for essentially the same reasons as claim 1 as presented, and since the "Oshima" reference does not cure the critical deficiencies of the background information and the "Bengtsson" reference, which were explained above. This is because any review of the secondary "Oshima" reference makes clear that it simply does not in any way disclose or suggest the claim 1 features, as explained above – nor is it asserted to do so. *Accordingly, claims 5 and 6 are allowable for the same reasons as claim 1 as presented, from which they depend.*

With respect to paragraph nine (9) of the Final Office Action, claim 9 was rejected under 35 U.S.C. § 103(a) as unpatentable over the purported "admitted prior art" (which is wrong as asserted) and the "Bengtsson" reference in view of U.S. Patent No. 6,535,811 ("Rowland").

Claim 9 depends from allowable claim 1 as presented – and therefore include all of the features of claim 1 as presented It is therefore respectfully requested that the obviousness rejections be withdrawn since claim 9 is allowable for essentially the same reasons as claim 1 as presented, and since the secondary "Rowland" reference does not cure the critical deficiencies of the background information and the "Bengtsson" reference, which were explained above – nor is asserted to do so. This is because any review of the "Rowland" reference makes clear that it simply does not in any way disclose or suggest the features of claim 1 as presented, as explained above. *Accordingly, claim 9 is allowable for the same reasons as claim 1 as presented from which it depends.*

It is therefore respectfully submitted that claims 1 to 14, as presented, are allowable.

Conclusion

It is therefore respectfully submitted that all of claims 1 to 14 are allowable. It is therefore respectfully requested that the rejections be withdrawn, since all issues raised have been addressed and obviated. An early and favorable action on the merits is respectfully requested.

Respectfully submitted,

Dated: 7/15/2006

By: _____
Gerard A. Messina
Reg. No. 35,952

KENYON & KENYON LLP
One Broadway
New York, New York 10004
(212) 425-7200

CUSTOMER NO. 26646

1207638

15